prototype

Version: 1.0
Register map hash: `0x593FA68E`

Thursday 1st January, 1970 00:00

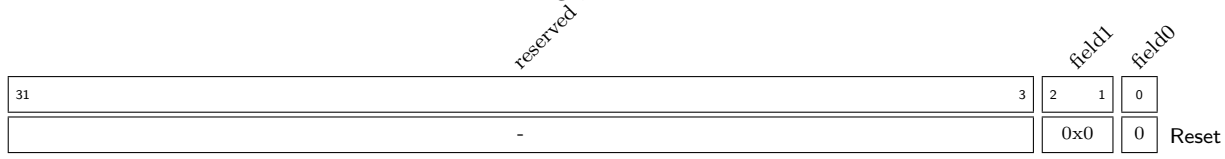
Comprehensive example exercising every v1 access mode, mirroring the prototype demo module (reg0..reg11).

1 Register List

#	Name	SW/HW	Address	Type	Width	Reset
0	reg0	RW/R	0x00000000	FIELDS	3	0x0
1	reg1	RO/W	0x00000004	FIELDS	6	0x0
2	reg2	WO/R	0x00000008	FIELDS	1	0x0
3	reg3	RW/NA	0x0000000C	FIELDS	8	0x0
4	reg4	RW/RW	0x00000010	FIELDS	9	0x0
5	reg5	RW/R	0x00000014	FIELDS	8	0x0
6	reg6	RW/R	0x00000018	FIELDS	12	0xF0
7	reg7	RW/R	0x0000001C	FIELDS	12	0xF0
8	reg8	RW/R	0x00000020	FIELDS	8	0xF
9	reg9	RW/R	0x00000024	FIELDS	8	0x0
10	reg10	RW/R	0x00000028	FIELDS	4	0x0
11	reg11	RW/R	0x0000002C	FIELDS	2	0x0

2 Registers

Register 2.1: REG0 - RW/R (0x00000000)
Plain rw storage, hardware reads back.

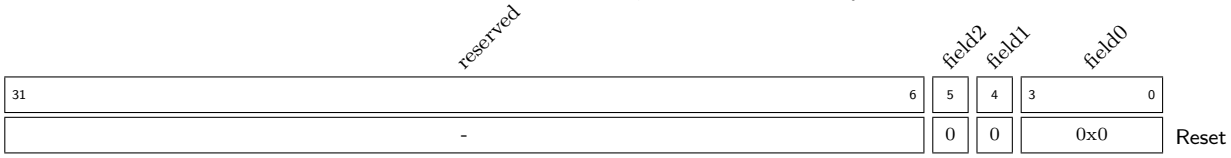


field0 (sw: rw, hw: r)

field1 (sw: rw, hw: r)

reserved Bits 31:3. Read as 0, writes have no effect.

Register 2.2: REG1 - RO/W (0x00000004)
Hardware-driven status, software read-only.



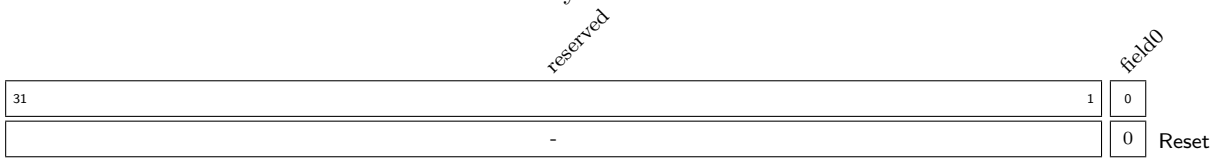
field0 (sw: ro, hw: w)

field1 (sw: ro, hw: w)

field2 (sw: ro, hw: w)

reserved Bits 31:6. Read as 0, writes have no effect.

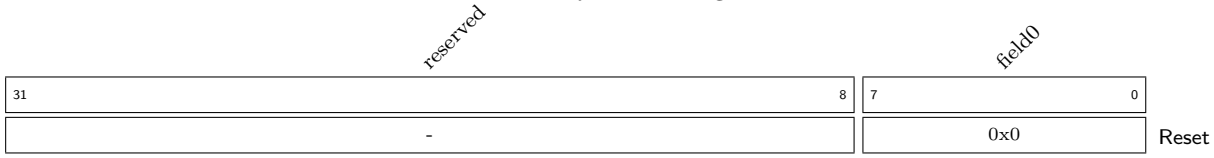
Register 2.3: REG2 - WO/R (0x00000008)
Write-only command field.



field0 (sw: wo, hw: r)

reserved Bits 31:1. Read as 0, writes have no effect.

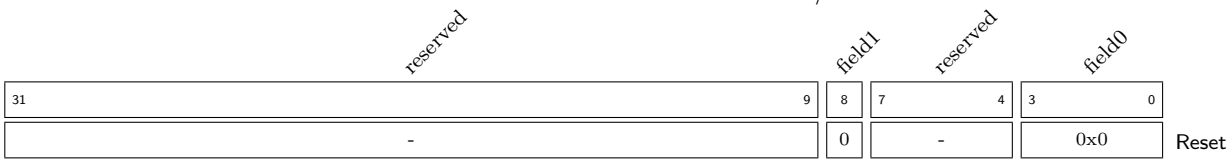
Register 2.4: REG3 - RW/NA (0x0000000C)
Software-only scratch register.



field0 (sw: rw, hw: na)

reserved Bits 31:8. Read as 0, writes have no effect.

Register 2.5: REG4 - RW/RW (0x00000010)
Hardware write-enable and hardware set/clear.



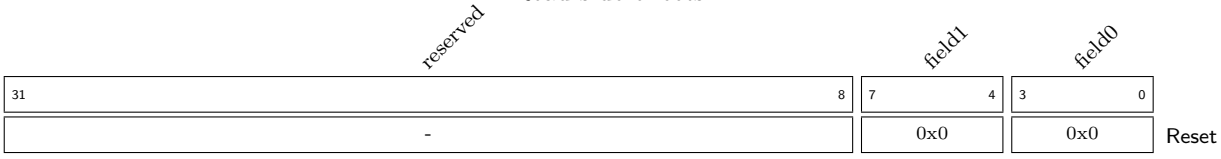
field0 (sw: rw, hw: rw)

reserved Bits 7:4. Read as 0, writes have no effect.

field1 (sw: rw, hw: r)

reserved Bits 31:9. Read as 0, writes have no effect.

Register 2.6: REG5 - RW/R (0x00000014)
Read side effects.

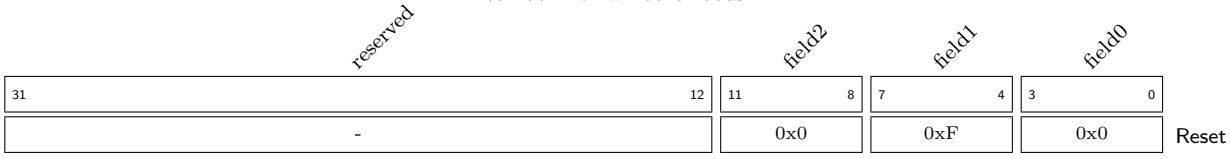


field0 (sw: rw, hw: r, onread: rclr)

field1 (sw: rw, hw: r, onread: rset)

reserved Bits 31:8. Read as 0, writes have no effect.

Register 2.7: REG6 - RW/R (0x00000018)
Write-1 onwrite effects.



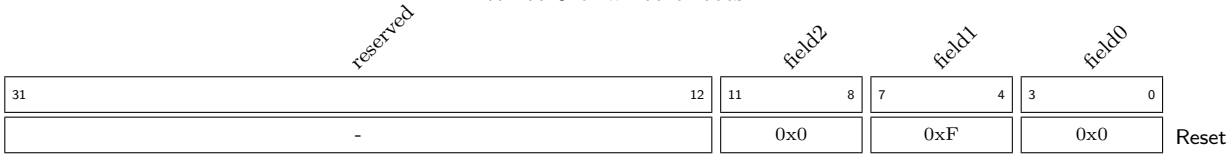
field0 (sw: rw, hw: r, onwrite: woset)

field1 (sw: rw, hw: r, onwrite: woclr)

field2 (sw: rw, hw: r, onwrite: wot)

reserved Bits 31:12. Read as 0, writes have no effect.

Register 2.8: REG7 - RW/R (0x0000001C)
Write-0 onwrite effects.



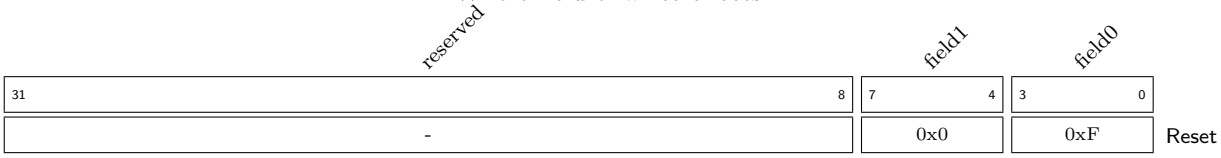
field0 (sw: rw, hw: r, onwrite: wzs)

field1 (sw: rw, hw: r, onwrite: wzc)

field2 (sw: rw, hw: r, onwrite: wzt)

reserved Bits 31:12. Read as 0, writes have no effect.

Register 2.9: REG8 - RW/R (0x00000020)
Whole-field onwrite effects.

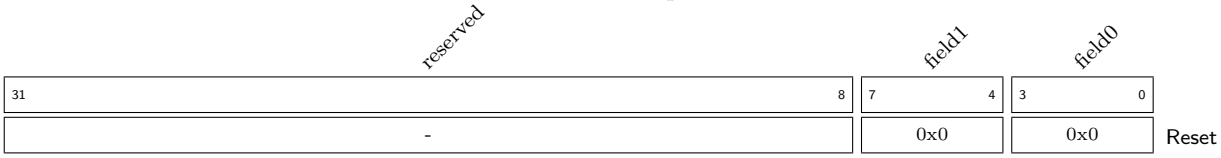


field0 (sw: rw, hw: r, onwrite: wclr)

field1 (sw: rw, hw: r, onwrite: wset)

reserved Bits 31:8. Read as 0, writes have no effect.

Register 2.10: REG9 - RW/R (0x00000024)
Software-access pulses.

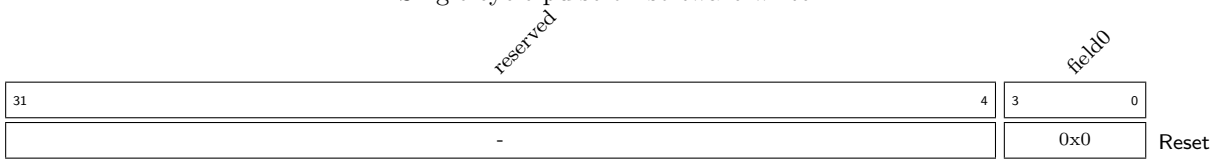


field0 (sw: rw, hw: r)

field1 (sw: rw, hw: r)

reserved Bits 31:8. Read as 0, writes have no effect.

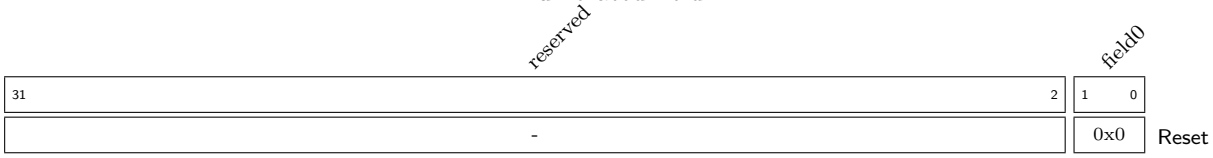
Register 2.11: REG10 - RW/R (0x00000028)
Single-cycle pulse on software write.



field0 (sw: rw, hw: r, singlepulse)

reserved Bits 31:4. Read as 0, writes have no effect.

Register 2.12: REG11 - RW/R (0x0000002C)
Enumerated field.



field0 (sw: rw, hw: r; values: STATE0=0, STATE1=1, STATE2=2, STATE3=3)

reserved Bits 31:2. Read as 0, writes have no effect.